WHAT IS CLAIMED IS:

1. A system, comprising:

a circuit; and

a regulator circuit operable to selectively provide a current supplied by a system power source to the circuit at a first current value and at a second current value.

2. The system according to claim 1, wherein the regulator circuit comprises a plurality of current sources.

3. The system according to claim 2, wherein at least one of the plurality of current sources is selectively activated by an enable signal.

4. The system according to claim 3, wherein the plurality of current sources form mirror branches of a current mirror.

5. The system according to claim 4, wherein the at least one of the plurality of current sources comprises a first transistor and a second transistor connected in series to the first transistor, wherein a control terminal of the first transistor is coupled to a control terminal of a transistor in a reference leg of the current mirror and a control terminal of the second transistor is coupled to the enable signal.

6. The system according to claim 3, further comprising a delay component responsive to the enable signal and operable to delay the activation of the at least one of the plurality of current sources relative to the enable signal being in an enabling state.

7. The system according to claim 6, wherein the delay component is coupled between the enable signal and the regulator circuit.

8. The system according to claim 6, wherein the delay component delays one of a rising edge and a falling edge of the enable signal by an amount that is greater than a delay of the other of the rising edge and the falling edge of the enable signal.

9. The system according to claim 1, wherein the circuit includes a memory device.

10. The system according to claim 9, wherein the memory device and the regulator circuit both receive an enable signal, the current value provided by the regulator circuit being based upon a value of the enable signal.

11. A system, comprising:

a circuit with an enable input for selectively enabling an operation to be performed in the circuit; and

a regulator circuit coupled between a system power source and the circuit and having a control input for controlling the amount of supply current available to the circuit wherein the enable input of the circuit and the control input of the regulator circuit are coupled one to the other.

12. The system according to claim 11, wherein the regulator circuit comprises a plurality of current sources, at least one of the plurality of current sources is activated by an enable signal coupled to the control input of the regulator circuit.

13. The system according to claim 12, wherein the plurality of current sources form mirror branches of a current mirror.

14. The system according to claim 12, wherein the at least one of the plurality of current sources is adapted for receiving the enable signal.

15. The system according to claim 12, further comprising a delay component operable to delay the deactivation of the at least one of the plurality of current sources relative to the circuit being disabled.

16. The system according to claim 15, wherein the delay component is coupled between the enable signal and the regulator circuit.

17. The system according to claim 15, wherein the delay component delays one edge of the enable signal relative to a second edge of the enable signal.

18. The system according to claim 12, wherein the at least one of the plurality of current sources comprise a first transistor and a second transistor connected in series to the first transistor, and a control terminal of the second transistor is coupled to the enable signal.

19. The system according to claim 11, wherein the circuit includes a memory device, and the enable input is a chip enable input of the memory device.

20. The system according to claim 19, wherein the memory device and the regulator circuit receive the same enable signal.

21. A method, comprising the steps of:

receiving an enable signal; and

supplying a current to a circuit having a current level that is based on a value of the enable signal.

22. The method according to claim 21, wherein the step of supplying the current further comprises the step of:

activating any one or more of a plurality of current sources in a regulator circuit so as to control the current supplied to the circuit, based on the value of the enable signal.

23. The method according to claim 22, wherein the step of supplying the current further comprises the step of delaying current source deactivation relative to the current source activation.

24. The method according to claim 21, further comprising the step of selectively enabling an operation in the circuit based on the value of the enable signal.

25. The method according to claim 24, further comprising the steps of delaying the step of supplying a current relative to the step of selectively enabling an operation.

26. The method according to claim 24, wherein the step of supplying the current further comprises the steps of:

supplying a first current level when the enable signal is a first value; and

supplying a second current level, different from the first current level, when the enable signal is a second value.

27. A method, comprising the steps of:

coupling a system power source to a circuit; and

selectively limiting the current supplied by the system power source to the circuit to any of at least two distinct non-zero current levels.

28. The method according to claim 27, wherein the step of selectively limiting the current comprises the steps of:

coupling a regulator circuit having a plurality of current sources between the system power source and the circuit, operable to supply the current to the circuit; and

selectively activating one or more of the plurality of current sources so as to limit the current supplied to the circuit to any of the at least two distinct non-zero current levels.

29. The method according to claim 28, wherein the step of selectively activating further comprises the steps of:

selectively activating the one or more of the plurality of current sources so as to limit the current supplied to the circuit to a first current level when an enable signal is a first value; and

selectively activating one or more of the plurality of current sources so as to limit the current supplied to the circuit to a second current level when the enable signal is a second value.

30. The method according to claim 28, further comprising the step of delaying the current source deactivation relative to the current source activation.

31. The method according to claim 27, further comprising the step of:

receiving an enable signal at the circuit for selectively enabling an operation by the circuit, wherein the distinct non-zero current level supplied by the system power source is based upon the enable signal.

32. The method according to claim 31, wherein the enable signal selectively enables a memory access operation to occur.